What is claimed is:

1. A method of operating a multiple-modulus prescaler having at least a modulus P and controlled by counting transitions of an applied frequency signal, comprising:

determining at least one of an integer portion Q and a remainder portion R of a division operation N/P, where a desired output frequency is N times an input reference frequency;

during at least a portion of a modulus control signal, alternating the modulus control signal between high and low states such that a maximum number of counts that the modulus control signal resides within a given state is less than R.

2. The method of Claim 1, further comprising toggling the modulus control signal between states at ~~each~~ count.

3. A multiple-modulus prescaler and associated control circuitry, operated by counting transitions of an applied frequency signal, comprising:

a first counter, including means for storing a first preset count, for counting transitions of the applied frequency signal; and

a second counter, including means for storing a second preset count, for counting transitions of the applied frequency signal;

wherein at least one of the counters, during counting of the preset count, generates an output signal that transitions multiple times.

4. A method of operating a multiple-modulus prescaler, comprising:

controlling selection between at least a first and second modulus on a cycle basis such that over the course of a cycle the prescaler divides an applied frequency signal by the first modulus for a first proportion of the

cycle and divides the applied frequency signal by the second modulus for a second proportion of the cycle; and

controlling selection between at least the first and second modulus on a subcycle basis such that over the course of a subcycle the prescaler divides the applied frequency signal by the first modulus for a first proportion of the subcycle and divides the applied frequency signal by the second modulus for a second proportion of the subcycle.

5. The method of Claim 4, wherein said cycle includes multiple subcycles.

6. A method of operating a phase locked loop that receives a reference frequency and produces a output frequency, the phase locked loop including a multiple-modulus prescaler, the method comprising the steps of:

determining for a desired output frequency a first proportion of a period, defined by the reciprocal of the input frequency, during which a first modulus is to be used, and determining a second proportion of the period during which a second modulus is to be used; and

controlling the modulus so as to change modulus a multiplicity of times during a period so as to obtain the desired output frequency.

7. A control circuit for a multiple-modulus prescaler, comprising:

a first counter that counts R total counts r at a time;

a second counter that counts Q total counts q at a time; and

a control circuit for repeatedly selecting in turn a first modulus for r counts and a second modulus for q counts.

8. A phase locked loop comprising:

a reference frequency signal;

a detector coupled to the reference frequency signal;

a loop filter coupled to an output signal of the detector;

a controlled oscillator coupled to an output signal of the loop filter, the controlled oscillator producing an output frequency signal; and

a frequency division circuit responsive to the output frequency signal for producing a feedback signal that is applied to the detector, the frequency division circuit comprising:

a multiple-modulus prescaler;

a first counter that counts R total counts r at a time;

a second counter that counts Q total counts q at a time; and

a control circuit for repeatedly selecting in turn a first modulus for r counts and a second modulus for q counts.